

**WHAT IS CLAIMED IS:**

1        1.    A system for reducing power consumption in digital  
2 circuits using charge redistribution, comprising:

3           - a plurality of signal lines;

4           - an intermediate floating virtual source/sink, and

5           a charge redistribution circuit connected to each said  
6 signal line that isolates said line from its source and connects  
7 it to the intermediate floating virtual source/sink during an  
8 idle period prior to a change of state.

1        2.    The system as claimed in claim 1 wherein the  
2 intermediate floating virtual source/sink comprises a charge  
3 storage element.

1        3.    The system as claimed in claim 1 wherein the charge  
2 redistribution circuit comprising the transition detector  
3 connected to the signal line having two outputs, one of which is  
4 connected to the input of a tri-state driver circuit and the  
5 other output simultaneously disable the tri-state driver  
6 circuit, and enables the control switch to connect its output to  
7 the floating source/sink whenever a transition is detected on a  
8 signal line.

1        4.    The system as claimed in claim 2 wherein the charge  
2 storage element is a capacitor or a set of capacitors.

1        5.    The system as claimed in claim 3 wherein the  
2 transition detector comprising a delay circuit having its input  
3 connected to the signal line and its output connected to the  
4 first output of the transition detector and to the first input  
5 of a 2-input exclusive-OR or exclusive-NOR gate while the second  
6 input of the exclusive-OR/ exclusive-NOR gate is directly  
7 connected to the signal line and its output is connected to the  
8 second output of the Transition Detector.

1        6.    The system as claimed in claim 4 wherein the capacitor  
2 comprising a floating conductor or a floating conducting mesh  
3 optionally coupled to capacitor elements.

1        7.    An integrated circuit for reducing power consumption  
2 in digital circuits using charge redistribution, comprising:

3            a plurality of signal lines;

4            an intermediate floating virtual source/sink, and

5            a charge redistribution circuit connected to each said  
6 signal line that isolates said line from its source and connects  
7 it to the intermediate floating virtual source/sink during an  
8 idle period prior to a change of state.

1        8.    An integrated circuit as claimed in claim 7 wherein  
2 the intermediate floating virtual source/sink comprises a charge  
3 storage element.

1        9.    An integrated circuit as claimed in claim 7 wherein  
2 the charge redistribution circuit comprising the transition  
3 detector connected to the signal line having two outputs, one of  
4 which is connected to the input of a tri-state driver circuit  
5 and the other output simultaneously disable the tri-state driver  
6 circuit and enables the control switch to connect its output to  
7 the floating source/sink whenever a transition is detected on a  
8 signal line.

1        10. An integrated circuit as claimed in claim 8 wherein  
2 the charge storage element is a capacitor or a set of  
3 capacitors.

1        11. An integrated circuit as claimed in claim 9 wherein  
2 the transition detector comprising a delay circuit having its  
3 input connected to the signal line and its output connected to  
4 the first output of the transition detects and to the first  
5 input of a 2-input exclusive-OR or exclusive-NOR gate while the  
6 second input of the exclusive-OR/ exclusive-NOR gate is directly  
7 connected to the signal line, its output is connected to the  
8 second output of the Transition Detector.

1        12. An integrated circuit as claimed in claim 10 wherein  
2 the capacitor comprises a floating conductor or a floating  
3 conducting mesh optionally coupled to capacitor elements.

1        13. A method for reducing power consumption in digital  
2 circuits using charge redistribution, comprising the steps of:

3            providing a plurality of signal lines;

4            providing an intermediate floating virtual  
5 source/sink, and

6            isolating each signal line from its source circuit and  
7 connecting it to the intermediate floating virtual source/sink  
8 during an idle period prior to a change of state.

1        14. The method as claimed in claim 13 wherein the step of  
2 providing an intermediate floating virtual source/sink  
3 comprising supplying a charge storage element.

1        15. The method as claimed in claim 13 wherein the change  
2 of state is identified by detecting a transition on the signal  
3 line.

1        16. The method as claimed in claim 14 wherein the charge  
2 storage element is supplied by connecting a capacitor or a set  
3 of capacitors.

1        17. The method as claimed in claim 15 wherein the  
2 transition is detected by exclusive-NORing or exclusive-ORing  
3 the signal with a delayed version of the signal.

1        18. The method as claimed in claim 15 wherein the signal  
2 line is connected to the intermediate floating virtual  
3 source/sink whenever a transition is detected.

1        19. The method as claimed in claim 16 wherein the  
2 capacitor is provided by a floating conductor or a floating  
3 conducting mesh optionally coupled to capacitor elements.